EMBEDDED JFETS FOR HIGH VOLTAGE APPLICATIONS

[0001] This application is a continuation of U.S. patent application Ser. No. 13/481,462, entitled "Embedded JFETS on High Voltage Applications," filed on May 25, 2012, which application is incorporated herein by reference.

BACKGROUND

[0002] Junction Field-Effect Transistor (JFET) is a type of field-effect transistor that can be used as an electronically-controlled switch or as a voltage-controlled resistor. In a JFET, electric charges flow through a semiconducting channel between a source and drain. By applying a bias voltage to a gate, the channel of the JFET may be pinched, so that the electric current flowing between the source and the drain is impeded or switched off.

[0003] JFETs have various structures. The different structures of the JFETs were design to suit for different usages of the JFETs. For example, the JFETs may be designed to be applied with high drain voltages, high currents, or the like.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0005] FIGS. **1**A through **4**C are top views and cross-sectional views of Junction Field-Effect Transistors (JFETs) in accordance with some exemplary embodiments; and

[0006] FIG. **5** illustrates an equivalent circuit diagram of the JFET shown in FIGS. **3**A through **4**C.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0007] The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are illustrative, and do not limit the scope of the disclosure.

[0008] A high voltage Junction Field-Effect Transistor (JFET) is provided in accordance with various exemplary embodiments. The variations and the operation of the embodiments are discussed. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements. In the illustrated embodiments, n-type JFETs are provided to explain the concept of the embodiments. It is appreciated that the teaching in the embodiments is readily available for the formation of p-type JFETs, with the conductivity types of the respective doped regions inverted.

[0009] FIGS. **1**A through **1**C are a top view and cross-sectional views of JFET **100** in accordance with some exemplary embodiments. Referring to FIG. **1**A, which is a top view, JFET **100** includes drain region **20**, gate electrode **24**, and source region **26**. Gate electrode **24** is disposed between drain region **20** and source region **26**. A plurality of contacts **30** are formed over and electrically couple to the respective underlying drain region **20**, gate electrode **24**, and source region **26**. Furthermore, High-Voltage N-Well (HVNW) **38**, P-Wells **40** (including **40**A and **40**B), and P-type Buried Layers (PBLs) **42** are also included in JFET **100**.

[0010] FIG. **1**B illustrates a cross-sectional view of JFET **100** as shown in FIG. **1**A, wherein the cross-sectional view is obtained from the plane crossing line **1**B-**1**B in FIG. **1**A. JFET **100** is formed over substrate **34**, which may be a p-type substrate, for example, although an n-type substrate may also be used. Buried N-Well (BNW) **36** is formed over substrate **34**. In some embodiments, BNW **36** is doped with an n-type impurity to an impurity concentration, for example, between about $10^{14}/cm^3$ and about $10^{17}/cm^3$. Over BNW **36**, HVNW **38** and PW regions **40** are formed. HVNW **38** and PW regions **40** may be doped with an n-type impurity and a p-type impurity, respectively, to impurity concentrations about $10^{14}/cm^3$ and about $10^{17}/cm^3$, for example. PBL **42** is formed under HVNW **38** and over BNW **36**, and is of p-type. The impurity concentration of PBL **42** may be between about $10^{15}/cm^3$ and about $10^{17}/cm^3$. Drain region **20** and source region **26** are heavily doped (represented by a "+" sign) n-type regions, which may have an n-type impurity concentration greater than about $10^{19}/cm^3$, or between about $10^{19}/cm^3$ and about $10^{21}/cm^3$.

[0011] Insulation region **46** is formed over HVNW **38**. In some embodiments, insulation region **46** is a field oxide region formed through the oxidation of silicon. In alternative embodiments, insulation region **46** may be a Shallow Trench Isolation (STI) region. A portion of PBL **42** is under and aligned to insulation region **46**. The formation of PBL **42** may be used for Reducing Surface electric Field (RESURF), which electric field may be high due to the high voltage applied on drain region **20**.

[0012] PW regions **40** include PW regions **40**A and PW **40**B, which are spaced apart from each other by portions of HVNW **38**, in which source region **26** is formed. As shown in FIG. **1**A, PW regions **40**A also includes PW regions **40**A**1**, **40**A**2**, and **40**A**3**, with each connected to one of PBLs **42**. Accordingly, when a voltage is applied to PW regions **40**A, the voltage may be applied to PBLs **42** through PWs regions **40**A. Referring to FIG. **1**B, in some embodiments, heavily doped p-type (P+) regions **48**A and **48**B are formed in PW regions **40**A and **40**B, respectively. P+ regions **48**A and **48**B act as the pickup regions of PW regions **40**A and **40**B, respectively. PW regions **40**A and **40**B may be electrically interconnected through overlying metal connections, and hence are at a same voltage level during the operation of JFET **100**.

[0013] Gate dielectric **22** and gate electrode **24** are formed over and aligned to HVNW **38**, insulation region **46**, and may extend over PW regions **40**A. In some embodiments, P+ region **48**A and gate electrode **24** are electrically interconnected through contact plugs **30** and one of metal lines **50**, so that the same voltage may be applied to gate electrode **24** and P+ regions **48**A, and hence to PW regions **40**A. Conductive feature **52**, which may be formed simultaneously when gate electrode **24** is formed, is over insulation region **46**, and may be electrically connected to drain region **20** through contact plugs **30** and one of metal lines **50**.

[0014] Referring to FIG. **1**B, it is observed that there is a current channel between and connected to drain region **20** and source regions **26**, wherein the current channel (illustrated as arrow **54**) is formed of n-type regions. A first current I**1** may flow through current channel **54** and between drain region **20** and source regions **26**. The current channel **54** includes the portion of HVNW **38** under drain region **20**, BNW **36** (which is under PBL **42**), and the portion of HVNW **38** between PW